REMARKS/ARGUMENTS

In the Office Action mailed October 22, 2007, claims 1-23 were rejected. Claims 1-23 have been resubmitted. Claims, 1, 14, 21, and 23 have been amended. Applicant hereby requests reconsideration of the application in view of the below-provided remarks.

Claim Rejections under 35 U.S.C. 112, second paragraph

Claims 4-7 are rejected under 35 U.S.C 112 second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 4, the Examiner notes:

> Claim 4 recites in part, "...a trigger circuit that activates the correction circuit when the predictor circuit contains a plurality of bits in which no erroneous bits have been detected." It is unclear why a correction circuit would be activated if no errors have been detected. If no errors are detected, there is no reason to correct an error.

In the Specification, paragraph [0015-0019], the Applicant describes the motivation for several elements of the invention, including the elements of claim 4. From paragraph [0015], the Applicant discloses, "A drawback of the PRBS error detector **150** [prior art] is that it assumes the portion of the PRBS stored in the seven-stage shift register contains no errors." From paragraph [0024], the Applicant discloses, "In one aspect of the invention, correcting the actual next bit is suppressed until no error has been detected in a plurality of bits in the sequence." Per paragraph [0017], this feature allows accurate bit error rate measurements of systems that have a high as well as low bit error rate performance.

Hence, in a bit sequence error detector, it is useful to determine if the shift register contains no errors, and the Applicant specifically defined this element as part of his invention. See paragraph [0061-0078]. Therefore, the elements of claim 4 are distinct, and supported by the Specification. Applicant respectfully requests that the rejection under 35 U.S.C. 112, second paragraph, be withdrawn.

Claims 5 – 7 are directly or indirectly dependent on claim 4. Applicant respectfully asserts that claims 5 – 7 are allowable at least based on an allowable base claim.

Claims 10 - 13 are rejected under 35 U.S.C 112 second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 10, the Examiner notes,

> Claim 10 recites in part ". . .a trigger circuit that activates the third logic element when the shift register contains a bit sequence in which no erroneous bits have been detected." However, the third logic element as detailed in claim 8 (claim 10 is dependent on claim 8), is as follows "a third logic element that receives the output signal and corrects the actual (N+l)-th bit according to the output signal as the (N+l)-th bit propagates through the shift register." As such, the third element when activated will be correcting data without errors.

The argument noted for Claim 4 above, also applies to Claim 10. Applicant respectfully requests that the rejection under 35 U.S.C. 112, second paragraph, be withdrawn.

Claims 11 – 12 are dependent on claim 10. Applicant respectfully asserts that claims 11 – 12 are allowable at least based on an allowable base claim.

Regarding Claim 13, the Examiner notes:

> Claim 13 recites in part "...a trigger circuit that prevents the third logic element from correcting any bits until the shift register contains a bit sequence in which no error has been detected." Again, it is unclear why correction would be performed on bits with no errors.

Again, the argument noted for Claim 4 above, also applies to Claim 13. Applicant respectfully requests that the rejection under 35 U.S.C. 112, second paragraph, be withdrawn.

Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 17, the Examiner notes:

> Claim 17 recites in part "...suppressing any correction of the actual next bit until no error has been detected in a plurality of bits in the sequence." It is unclear why a correction would be necessary if no error has been detected in the bit sequence.

Again, the argument noted for Claim 4 above, also applies to Claim 17. Applicant respectfully requests that the rejection under 35 U.S.C. 112, second paragraph, be withdrawn.

Claim Rejections under 35 U.S.C 102(e)

Claims 1-3, 8-9, 14-16, 18-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Reberga (U.S. Publication No. 200410128603). In response, Applicant has amended independent claims 1, 14, and 21 and respectfully submits that these claims are patentable over Reberga for the reasons provided below. Applicant argues that claim 8 does not anticipate Reberga, and has provided appropriate remarks, and respectfully submits that this claim is patentable over Reberga. The remaining claims depend directly or indirectly on independent claims 1, 8, 14 or 21. Therefore, Applicant respectfully submits that these claims are patentable.

Independent Claim 1

Claim 1 has been amended to particularly point out that the correction circuit corrects any error in the actual next bit to provide a corrected actual next bit "regardless of the statistical distribution of erroneous bits in the bit sequence." Support for this amendment is found in Applicant's Specification at, for example, paragraphs [0019] and [0020]. As amended, claim 1 recites:

> A bit error detection circuit comprising:
>
> a predictor circuit that uses a plurality of bits of a bit sequence to predict a next bit in the sequence;
>
> a comparator circuit that compares an actual next bit in the sequence with the predicted next bit to determine whether there is any error in the actual next bit; and
>
> a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit, regardless of the statistical distribution of erroneous bits in the bit sequence.

Applicant asserts that amended claim 1 is not anticipated by Reberga for the following reason:

Reberga does not disclose the statistical distribution of errors and their impact on the performance of the error detector

Reberga does not disclose any details related to the performance of the error detector. Specifically, Reberga does not disclose, "a correction circuit that corrects **any error** in the actual next bit to provide a corrected actual next bit, **regardless of the statistical distribution of erroneous bits in the bit sequence.**" (emphasis added). Therefore, Applicant asserts that claim 1 is not anticipated by Reberga.

As an additional comment, Applicant discloses several problems with the performance of error detectors in the prior art. Per Paragraph [0015], Applicant discloses, "A drawback of the PRBS error detector **150** (Fig.3 (prior art)) is that it assumes the portion of the PRBS stored in the seven-stage shift register contains no errors". Further, Applicant notes that error detector **150** is equivalent to Reberga's invention disclosure, as represented by Fig 3A of Reberga. Hence, Applicant's critique of the performance of the prior art error detector (paragraph [0015-0019]) is a direct critique of the Reberga invention, represented at least by Fig 3A of Reberga.

Independent Claims 14 and 21

Independent claims 14 and 21 have been amended to include similar limitations to claim 1. In view of the similarities between claims 14 and 21 and claim 1, Applicants assert that the remarks provided above in regard to claim 1 apply also to claims 14 and 21. Accordingly, Applicant respectfully asserts that independent claims 14 and 21 are not anticipated by Reberga.

Dependent Claims 2 – 3, 15 – 16, 18 – 20 and 22

Claims 2 – 3 are dependent on claim 1, claim 15 – 16 and 18 are dependent on claim 14, claims 19 – 20 are dependent on claim 18, and claim 22 is dependent on claim 21. Applicant respectfully asserts that claims 2 – 3, 15 – 16, 18 - 20 and 22 are allowable at least based on allowable base claims.

Independent Claim 8

Claim 8 recites:

A bit error detection circuit comprising:

a shift register that receives N bits of a pseudo-random bit sequence (PRBS);

a first logic element that receives output signals from two stages of the shift register and provides a signal indicative of a predicted (N+1)-th bit;

a second logic element that receives the signal indicative of the predicted (N+1)-th bit and a signal indicative of an actual (N+1)-th bit and provides an output signal indicative of any error in the actual (N+1)-th bit; and

a third logic element that receives the output signal and corrects the actual (N+1)-th bit according to the output signal as the (N+1)-th bit propagates through the shift register.

Applicant asserts that claim 8 is not anticipated by Reberga for the following reason:

Reberga does not disclose "a first logic element that receives output signals from two stages of the shift register....".

The Applicant's claim for "a first logic element" refers to element **440** in the embodiment of Fig.4 and element **640** in the embodiment of Fig. 6. In both embodiments, the first logic element receives output signal from two stages of the shift register. By comparison, in Reberga, Fig. 3A, 3B, 3C, 3D, the equivalent first logic element is block **14.** In Reberga, the first logic element receives output signals from only one stage of the shift register. There are no additional embodiments suggested by Reberga. Therefore, Applicant asserts that claim 8 is not anticipated by Reberga.

Dependent Claim 9

Claims 9 is dependent on claim 8. Applicants respectfully assert that claim 9 is allowable at least based on allowable base claims.

Claim Rejections under 35 U.S.C 103(a)

Claim 23 was rejected under 35 U.S.C. 103(a) as being unpatentable over Reberga (U.S. Publication No. 200410128603), in view of Rakib et al. (U.S. Publication No. 2001/0001616, hereinafter Rakib). In response, Applicant has amended claim 23 and respectfully submits that this claim is patentable over Reberga in view of Rakib for the reasons provided below:

Independent Claim 23

Claim 23 has been amended to particularly point out that "an input to the transmitter is an output of the pseudo-random sequence generator." Support for this amendment is found in Applicant's specification at, for example, Fig.1.

Claim 23 has also been amended to particularly point out that the correction circuit corrects any error in the actual next bit to provide a corrected actual next bit "regardless of the statistical distribution of erroneous bits in the bit sequence." Support for this amendment is found in Applicant's specification at, for example, paragraphs [0019] and [0020]. As amended, claim 23 recites,

> A high-speed communications system, comprising:
> a pseudo-random bit sequence generator for creating a pseudo-random bit sequence;
> a transmitter in signal communication with the pseudo-random bit sequence generator, wherein an input to the transmitter is an output of the pseudo-random sequence generator;
> a communications channel in signal communication with the transmitter, the transmitter for transmitting the pseudo-random bit sequence over the communications channel; and
> a pseudo-random bit sequence error detector, in signal communication with the communications channel, for detecting and correcting any error in an actual next bit of the pseudo-random bit sequence, wherein the pseudo-random bit sequence error detector comprises:
> a predictor circuit that uses a plurality of bits of the pseudo-random bit sequence to provide a predicted next bit of the pseudo-random bit sequence;
> a comparator circuit that compares the actual next bit in the pseudo-random bit sequence with the predicted next bit to determine whether there is an error in the actual next bit; and
> a correction circuit that corrects any error in the actual next bit to provide a corrected actual next bit, regardless of the statistical distribution of erroneous bits in the bit sequence.

Neither Reberga or Rakib disclose the statistical distribution of errors in a bit sequence and their impact on the performance of the bit sequence error detector

Reberga does not disclose any details related to the performance of the error detector. See discussion related to claim 1 for a detail discussion of this point.

Rakib discloses error detection and pseudo random bit sequences, but only in the context of a CDMA receiver and transmitter. These disclosures are not relevant to an error detector for a bit sequence at a baseband level of a communication system. For example, in reference to the Applicant's prior art, Fig. 1, the elements disclosed by Rakib relate to the TRANSMITTER **110** and/or RECEIVER **130**, and not to the PRBS ERROR DETECTOR **150**. Hence, Rakib does not disclose the statistical distribution of errors in a bit sequence and their impact on the performance of the bit sequence error detector.

Accordingly, the cited references fail to teach or suggest the specific combination recited in amended claim 23. Therefore, the Applicant respectively asserts that amended claim 23 is patentable over Reberga in view of Rakib.

CONCLUSION

Applicant respectfully requests reconsideration of the claims in view of the amendments and the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3718** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3718** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

/mark a. wilson/

Date: January 22, 2008

Mark A. Wilson
Reg. No. 43,994

Wilson & Ham
PMB: 348
2530 Berryessa Road
San Jose, CA 95132
Phone: (925) 249-1300
Fax: (925) 249-0111